CLAIMS

What is claimed is:

Sub A4

1. An apparatus comprising:

a predictor having a collision history table (CHT);

an extended load buffer coupled to the predictor;

a marking unit coupled to the extended load buffer;

a comparing unit coupled to the extended load buffer; and

a recovery unit coupled to the extended load buffer, wherein unexecuted load instructions are advanced over silent store instructions.

2. The apparatus of claim 1, wherein the predictor is a silent store predictor.

3. The apparatus of claim 2, wherein the silent store predictor uses path based indexing and the path is based on branches.

4. The apparatus of claim 3, wherein the silent store predictor is coupled with a state machine.

5. The apparatus of claim 4, wherein the state machine is one of a 1-bit, a 2-bit and a sticky bit.

6. The apparatus of claim 1, wherein the predictor is memory dependent.

7. The apparatus of claim 1, wherein the extended load buffer comprises

Cont A4

bit fields to mark load address match, load data match, load predict, and load flush, and bit fields for load address, load attribute and load data.

8. The apparatus of claim 1, wherein the CHT is one of indexed by a tag and tagless.

9. The apparatus of claim 1, wherein the CHT includes distance bits.

10. A system comprising:

a processor having internal memory,

a bus coupled to the processor;

a memory coupled to a memory controller and the processor;

wherein the processor includes a predictor having a collision history table (CHT);

an extended load buffer coupled to the predictor;

a marking unit coupled to the extended load buffer;

a comparing unit coupled to the extended load buffer; and

a recovery unit coupled to the extended load buffer, wherein unexecuted load instructions are advanced over store instructions.

11. The system of claim 10, wherein the predictor is a silent store predictor.

12. The system of claim 11, wherein the silent store predictor uses path based indexing and the path is based on branches.

A4

13. The system of claim 12, wherein the silent store predictor is coupled with a state machine.

14. The system of claim 13, wherein the state machine is one of a 1-bit, a 2-bit and a sticky bit.

15. The system of claim 10, wherein the predictor is memory dependent.

16. The system of claim 10, wherein the extended load buffer comprises

bit fields to mark load address match, load data match, load predict, and load flush, and bit fields for load address, load attribute and load data.

17. The system of claim 10, wherein the CHT is one of indexed by a tag and tagless.

18. The system of claim 10, wherein the CHT includes distance bits.

19. A method comprising:

fetching an instruction and determining if an instruction is one of a store and a load;

performing a silent store prediction if the instruction is a store;

executing the store instruction;

comparing an address and data of the store with load instructions in an extended load buffer;

A4

setting marking bits in an extended load buffer if a match is found in the comparing;

updating a memory with store instruction if the store instruction can be retired; and

bypassing a predicted silent store instruction and executing the load instruction if the instruction is a load.

20. The method of claim 19, further comprising

preparing the load instruction for retirement, and marking the load instruction flush in the extended load buffer.

21. The method of claim 19, wherein the predicting includes marking bits in a collision history table (CHT).

22. The method of claim 19, wherein the memory is a cache.

23. A program storage device readable by a machine comprising instructions that cause the machine to:

fetch an operation and determining if the operation is one of a store and a load;

perform a silent store prediction if the operation is a store;

execute the store operation;

compare an address and data of the store operation with load operations in an extended load buffer;

set marking bits in an extended load buffer if a match is found in the compare instruction;

A4

update a memory with a store operation if the store operation can be retired; and

bypass a predicted silent store operation and execute the load operation if the operation is a load.

24. The program storage device of claim 23, wherein the instructions further cause the machine to prepare the load operation for retirement, and mark the load operation flush in the extended load buffer.

25. The program storage device of claim 23, wherein the instruction that causes the machine to predict silent stores includes an instruction that causes the machine to mark bits in a collision history table (CHT).

26. The program storage device of claim 23, wherein the memory is a cache.